Status Report #1 – 2/25/2017

Circuit creation works and so does truth table generation. Loading and saving workings. I’ve been working on the timing diagram and just added a clear button so that the diagram can be reset.

Status Report #2 – 4/03/2017

Overhauled internal logic simulation. Switched from iterating through the entire tree multiple times (very inefficient) to using a distributed network with a fast update cycle. This has fixed all the simulation bugs, but the processor overhead is higher now.

Status Report #3 – 4/20/2017

Only a bit left to do. I’m going to focus on building up a component library, Implementing the ability to make lines at right angles, and also making builds for all target systems.